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PTO/SB/05 (4/98)  
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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. 00-264

First Inventor or Application Identifier Feng Qian

Title Frame Matching Method

Express Mail Label No. FT643645225TTS

## APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1.  \* Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2.  Specification [Total Pages 13]
  - Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3.  Drawing(s) (35 U.S.C. 113) [Total Sheets 4]
4. Oath or Declaration [Total Pages 2]
  - a.  Newly executed (original or copy)
  - b.  Copy from a prior application (37 C.F.R. § 1.63(d))  
(for continuation/divisional with Box 16 completed)
    - i.  DELETION OF INVENTOR(S)  
Signed statement attached deleting  
inventor(s) named in the prior application,  
see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

\*NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

ADDRESS TO: Assistant Commissioner for Patents  
Box Patent Application  
Washington, DC 20231

5.  Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)
  - a.  Computer Readable Copy
  - b.  Paper Copy (identical to computer copy)
  - c.  Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

7.  Assignment Papers (cover sheet & document(s))
8.  37 C.F.R. § 3.73(b) Statement  Power of  
(when there is an assignee)  Attorney
9.  English Translation Document (if applicable)
10.  Information Disclosure Statement (IDS)/PTO-1449  Copies of IDS  
Citations
11.  Preliminary Amendment
12.  Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)
13.  \* Small Entity Statement(s)  Statement filed in prior application,  
(PTO/SB/09-12)  Status still proper and desired
14.  Certified Copy of Priority Document(s)  
(if foreign priority is claimed)
15.  Other: Cover Letter

16. If a CONTINUATING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

Continuation  Divisional  Continuation-in-part (CIP)

of prior application No: 60 / 209,490 Provisional App

Prior application information: Examiner \_\_\_\_\_

Group / Art Unit: \_\_\_\_\_

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

## 17. CORRESPONDENCE ADDRESS

Customer Number or Bar Code Label



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Name (Print/Type)	Bruce Hopenfeld	Registration No. (Attorney/Agent)	39,714
Signature	mc Hopenfeld	Date	9/29/2006

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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

## In re Application of :

Feng Qian

For : Frame Matching Method

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington D C 20231, on the date indicated below:

Christopher Leach

Date

Signature

Atty Docket : 00-264



## TRANSMITTAL LETTER FOR PATENT APPLICATION

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir,

The following paper(s) and/or fee(s) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee", addressed to :

Box Patent Application  
Assistant Commissioner for Patents  
Washington, D.C. 20231

1. Fee Transmittal Form (in duplicate).
2. Patent Application comprising the following :
  - a. Specification, pages = 0
  - b. Drawing, sheets = 0
  - c. Assignment and declaration with power of attorney.

It is respectfully requested that the Commissioner accord the enclosed patent application a filing date and a serial number.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

LSI Logic Corporation  
1551 McCarthy Blvd., MS D-106  
Milpitas, CA 95035  
408/433-7191

Date: Sept. 29, 2000

Respectfully submitted,

Bruce Hopenfeld

Reg. No. 39,714

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# FEE TRANSMITTAL

## for FY 2000

Patent fees are subject to annual revision.

Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT (\$)

## Complete if Known

Application Number	60/209,490
Filing Date	6/7/00
First Named Inventor	Feng Qian
Examiner Name	N/A
Group / Art Unit	N/A
Attorney Docket No.	00-264

## METHOD OF PAYMENT (check one)

1.  The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number **12-2252**Deposit Account Name **LSI LOGIC CORPORATION** Charge Any Additional Fee Required  
Under 37 CFR §§ 1.16 and 1.17

- 2.
- 
- Payment Enclosed:

 Check     Money     Other

## FEE CALCULATION

## 1. BASIC FILING FEE

Large Entity Small Entity  
Fee Fee Fee Fee Fee Description

Code (\$)	Code (\$)	Fee Paid
101	690	201 345 Utility filing fee
106	310	206 155 Design filing fee
107	480	207 240 Plant filing fee
108	690	208 345 Reissue filing fee
114	150	214 75 Provisional filing fee

SUBTOTAL (1) (\$)**690**

## 2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
9	-20** =	X	= 0
Independent Claims	1 - 3** =	X	= 0
Multiple Dependent		0	= 0

\*\*or number previously paid, if greater; For Reissues, see below

## Large Entity Small Entity

Fee Fee Fee Fee Fee Description

Code (\$)	Code (\$)	Fee Paid
103	18	203 9 Claims in excess of 20
102	78	202 39 Independent claims in excess of 3
104	260	204 130 Multiple dependent claim, if not paid
109	78	209 39 ** Reissue independent claims over original patent
110	18	210 9 ** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$)**0.00**

## 3. ADDITIONAL FEES

Large Entity	Small Entity	Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
105	130	205 65		Surcharge - late filing fee or oath	
127	50	227 25		Surcharge - late provisional filing fee or cover sheet	
139	130	139 130		Non-English specification	
147	2,520	147 2,520		For filing a request for reexamination	
112	920*	112 920*		Requesting publication of SIR prior to Examiner action	
113	1,840*	113 1,840*		Requesting publication of SIR after Examiner action	
115	110	215 55		Extension for reply within first month	
116	380	216 190		Extension for reply within second month	
117	870	217 435		Extension for reply within third month	
118	1,360	218 680		Extension for reply within fourth month	
128	1,850	228 925		Extension for reply within fifth month	
119	300	219 150		Notice of Appeal	
120	300	220 150		Filing a brief in support of an appeal	
121	260	221 130		Request for oral hearing	
138	1,510	138 1,510		Petition to institute a public use proceeding	
140	110	240 55		Petition to revive - unavoidable	
141	1,210	241 605		Petition to revive - unintentional	
142	1,210	242 605		Utility issue fee (or reissue)	
143	430	243 215		Design issue fee	
144	580	244 290		Plant issue fee	
122	130	122 130		Petitions to the Commissioner	
123	50	123 50		Petitions related to provisional applications	
126	240	126 240		Submission of Information Disclosure Stmt	
581	40	581 40		Recording each patent assignment per property (times number of properties)	
146	690	246 345		Filing a submission after final rejection (37 CFR § 1.129(a))	
149	690	249 345		For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) _____					
Other fee (specify) _____					

Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$)**0.00**

## SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Bruce Hopenfeld	Registration No. (Attorney/Agent)	39,714	Telephone	(408) 433-8000
Signature	<i>Bruce Hopenfeld</i>			Date	9/29/2006

## WARNING:

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: Qian )  
                                  ) Group Art Unit: Not Assigned  
                                  )  
Serial No.: Not Assigned    ) Examiner: Not Assigned  
                                  )  
Filed: June 6, 2000           ) Atty. Docket No.: 00-264  
                                  )  
For: Frame Matching Method    )  
                                  )  
                                  )  
                                  )

**PRELIMINARY AMENDMENT**

Hon. Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Sir:

Before a first Office Action in the above captioned case, please amend the above captioned case as follows:

**In the Specification**

On page 8, line 14, please delete “[I threw this in for fun.]”.

**In the Claims**

In claim 5, line 1, please delete “each of”.

In claim 5, lines 1 and 2, please change “N” to --X--.

In claim 6, line 1, please change “Error! Reference source not found.” to --1--.

In claim 7, line 1, please change “Error! Reference source not found.” to --1--.

**In the Abstract:**

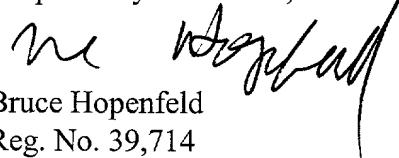
Please insert: “The present invention pertains to a frame matching method for digital systems. Excess bits are deleted from a frame of data in a single iteration through the data, thereby creating a reduced length frame, wherein the deleting step is performed such that the distance between any two consecutive deleted bits within any group within a first subset of the frame is A bits, and the distance between any two consecutive deleted bits within any group within a second subset of the frame is B bits, where A is an integer

greater than 0 and B is an integer greater than A, and where the first subset and the second subset together form a plurality of consecutive bits."

Summary

The attorney below, who will now be responsible for prosecuting this application, can be contacted at LSI Logic Corporation, Milpitas, CA, 408-433-6100 (direct dial).

Respectfully Submitted,

  
Bruce Hopenfeld  
Reg. No. 39,714

Date: September 29, 2000

PATENT

Docket: 00-264

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Chris Gleach

[NAME OF PARALEGAL]

### Frame Matching Method

By:

Feng Qian  
25851 Majorca Way  
Mission Viejo, CA 92692  
Citizenship: U.S.

## **BACKGROUND OF THE INVENTION**

### Field of the Invention

This invention relates to frame based digital communication systems and more  
5 particularly to a method for processing frames having a certain size in systems configured  
for frames having a different size.

### Description of the Related Art

Digital data is often communicated in frames, which are groups of digital data that  
10 are processed together, as will be further described below. Often, it is desired to send or  
receive frames having a certain size in systems configured for different sized frames. For  
example, in the IS2000.2-A standard for code division multiple access (CDMA)  
communications, encoded symbols at a rate of L symbols per frame must be matched  
with a transmission scheme that processes N symbols per frame, where N is greater than  
15 L. In this case, for any one frame, the L symbols are repeated M times, where M is the  
smallest integer such that  $ML > N$ . Then, the ML symbols are reduced to N symbols by  
deleting (puncturing) P symbols, where  $P = ML - N$ . There is no appreciable loss of  
information since in CDMA, many symbols are redundant to provide robust protection  
against transmission errors; deleting a few redundant symbols will typically not cause any  
20 significant problems, especially if the symbols are far apart.

A system designer must decide which symbols to puncture. One conventional  
choice would be to simply puncture out every  $LM/P$  symbols. Since the symbols are  
discrete, in practice this means that the nearest integer lower than  $LM/P$  is punctured. For  
25 example,  $LM$  is 300 and  $P$  is 100 (i.e. 100 symbols must be deleted), every third symbol  
may be punctured. Using more realistic numbers for CDMA,  $LM$  may be 2400 and  $P$   
864, so that every other symbol is punctured. However, if every other symbol is  
punctured starting at the beginning of the frame, there will be 672 ( $=2400 - 2 * 864$ )  
consecutive symbols at the end of the frame that aren't punctured at all. This non-

uniformity in the puncturing scheme may result in performance degradation since, as mentioned above, it is desirable to keep the distance between deleted symbols as great as possible.

5 An alternate scheme involves puncturing out every D1th symbol, where D1 is the nearest integer greater than  $LM/P$ , thereby puncturing P1 symbols. In this case, if not enough symbols have been punctured (i.e.  $P1 < P$ ), a second iteration is performed to puncture  $P2 (=P-P1)$  symbols that are  $D1 * \lfloor P1/P2 \rfloor$  symbols apart. (Here, the underline denotes the nearest integer less than the amount in brackets.) Returning to the above  
10 example, in the first pass, every third symbol would be deleted, resulting in the deletion of 800 symbols. After this pass, 64 symbols still must be deleted, which is done by deleting every 36<sup>th</sup> symbol. This second puncturing scheme is more uniform than the first scheme described above. However, this second puncturing scheme requires two iterations, which may be undesirable from an implementation standpoint. Further, this  
15 second scheme may result in two consecutive symbols being punctured, which could result in performance degradation. [Has this been publicly disclosed by Samsung? If not, we need its permission to discuss here.]

Therefore, it would be desirable to have a more uniform puncturing scheme than  
20 the first scheme without the complications and problems associated with the second scheme.

## **SUMMARY OF THE INVENTION**

According to the present invention, excess bits are deleted from a frame of data in a single iteration through the data, thereby creating a reduced length frame, wherein the  
5 deleting step is performed such that the distance between any two consecutive deleted bits within any group within a first subset of the frame is A bits, and the distance between any two consecutive deleted bits within any group within a second subset of the frame is B bits, where A is an integer greater than 0 and B is an integer greater than A, and where the first subset and the second subset together form a plurality of consecutive bits.

10

434532572E a 44P3 A 43343

## BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading  
the following detailed description and upon reference to the accompanying drawings in  
5 which:

Figure 1 is a block diagram of a possible digital communication system that  
includes a frame matching circuit the implements a frame matching method according to  
10 the present invention.

Figure 2 is a flow chart of a first possible frame matching method according to the  
present invention.

Figure 3 is a flow chart of a second possible frame matching method according to  
the present invention.

15 Figure 4 is a flow chart of a second possible frame matching method according to  
the present invention.

While the invention is susceptible to various modifications and alternative forms,  
specific embodiments thereof are shown by way of example in the drawings and will  
20 herein be described in detail. It should be understood, however, that the drawings and  
detailed description thereto are not intended to limit the invention to the particular form  
disclosed, but on the contrary, the intention is to cover all modifications, equivalents and  
alternatives falling within the spirit and scope of the present invention as defined by the  
 appended claims.

## **DETAILED DESCRIPTION OF THE INVENTION**

This specification describes frame matching methods in the context of CDMA  
5 systems. However, it will be appreciated that the present invention is not restricted to  
CDMA systems.

As used herein, a “subset” of a frame consists of at least one group of consecutive  
bits within a frame. For example, in a frame with bits ordered 1 through 10, a subset of  
10 the frame may consist of a group of the first two bits of the frame and a group of the last  
three bits of the frame. Another subset of that frame may consist of the third through  
seventh bits of the frame. If reference to more than one subset is made, such subsets are  
assumed not to overlap with one another. The length of a subset or group is the number  
of bits within the subset or group. A subset has a length of at least one (there are no  
15 “null” subsets).

The “distance” between two bits is the number of bits that separate those bits in an  
ordered frame. For example, in a frame with bits ordered 1 through 10, the distance  
between the first bit and the third bit is 1.

20 “Consecutive deleted bits” means a pair of deleted bits that are not separated by  
any other deleted bit.

Figure 1 represents a digital communications system 140 within which the present  
25 invention may be embodied. As shown, the digital system 140 comprises a discrete-time  
channel 142 interposed between an encoder 144 and a decoder 130. Discrete-time  
channel 142 comprises a modulator 146, a channel 148 and a demodulator 150. An  
interleaver 145 is interposed between the encoder 144 and the modulator 146. A  
deinterleaver 151 is interposed between the decoder 130 and the demodulator 150.

Channel 148 may be a transmission channel or a storage medium being written to and read from. Interleaver 145 receives a digital output signal from a rate matching circuit 147, which in turn receives a digital signal from an encoder 144. The interleaver 145 interleaves this digital output signal over a certain time period, which is usually 5 predetermined and known as a frame. Modulator 146 serves to translate the digital output signal from interleaver 145 into signals suitable for channel 148 and thereafter drives the signals across channel 148.

Channel 148 may suffer from interference that corrupts said signals, the 10 interference possibly taking form in any combination of additive noise, cross channel interference, multi-path interference, and channel fading. Demodulator 150 serves to receive the signals from channel 148 while minimizing the interference as much as is practical, and thereafter translate the signals into digital signals for input to deinterleaver 151, which deinterleaves the digital signal and provides it to decoder 130. Discrete-time 15 channel 142 can thus be viewed as a unit accepting digital input signals and producing possibly corrupted digital output signals although the present invention is not limited to noisy channels.

Encoder 144 is a convolutional encoder which serves to add redundancy to input 20 data signal 152. The output of the encoder 144 is L symbols per frame, which must be matched with the interleaver 145, which interleaves N symbols per frame, where N is greater than L. This matching is performed by the rate matching circuit 147, which repeats the L symbols of an input frame M times, where M is the smallest integer such that  $ML > N$ . Thereafter, the matching circuit 147 punctures P symbols from the repeated 25 input frame, where  $P = ML - N$ .

According to the present invention, the matching circuit 147 deletes bits in a single iteration through a frame such that the distance that separates consecutive deleted bits is either A or B, where A is an integer greater than 0 and B is an integer greater than

A. Preferably, A is equal to D-1, where D is the greatest integer less than LM/P, where P=LM-N. In this case, B is preferably equal to A+1. For example, if N=1536 bits and L=1200 bits, then M equals 2, D is equal to 2, A is equal to 1 and B is equal to 2. Thus, either 1 or 2 bits separate deleted bits, which results in relatively uniform puncturing.

- 5 The number of deleted bits  $P_{D+1}$  separated by B is preferably equal to LM-PD and the number of deleted bits separated by A ( $P_D$ ) is preferably equal to P- $P_{D+1}$ . As will be described below, there are various implementations of the above described method.

More formally, according to the present invention, LM-N bits are deleted from a  
10 frame of data in a single iteration through the data, thereby creating a reduced length frame, wherein the deleting step is performed such that the distance between any two consecutive deleted bits within any group within a first subset of the frame is A bits, and the distance between any two consecutive deleted bits within any group within a second subset of the frame is B bits, where A is an integer greater than 0 and B is an integer  
15 greater than A, and where the first subset and the second subset together form a plurality of consecutive bits.

Preferably, an entire frame is punctured according to the preferred values of A and B. However, a subset of a frame may be punctured with these (or other) values of A and  
20 B and the remainder of the frame may be punctured by other known methods. For example, the first two bits of a frame may be punctured, and then the remainder of the frame may be punctured with the minimum distance between punctured bits as A or B; the total number of punctured bits should add up to P.

25 As described above, there are many different implementaions of the high level method described above. According to one implementation, every D+1th bit is deleted in a frame until  $P_{D+1}$  bits have been deleted. Then, every Dth bit is deleted until the entire frame has been processed. This method will be described in Figure 2. A more uniform scheme involves alternating between deleting every D+1th bit and deleting every Dth bit

until either  $P_{D+1}$  bits separated by B have been deleted or  $P_D$  bits separated by A have been deleted. Thereafter, if the former is true, every Dth bit is deleted, or, if the latter, every  $D+1$ th bit is deleted. This method will be described in Figure 3. According to a third yet still more unfirom method, to be described in Figure 4, the following pattern of deletions  
5 is repeated: 1 symbol is deleted after skipping A symbols, N symbols separated by B symbols are then deleted, 1 symbol is deleted after skipping A symbols, and then O symbols separated by B symbols are then deleted, where N is the nearest integer less than  $P_{D+1}/ P_D$  and O is equal to  $N + 1$ . For example, if A is 1, B is 2, N is 3 and O is 4, then the following bits are deleted 1, 3, 6, 9, 12, 14, 17, 20, 23, 26, 28 ...

10

Still according to another method, the following pattern of deletions is repeated: N symbols separated by A symbols are deleted and O symbols separated by B symbols are deleted, where  $N:O$  is equal to  $P_D : P_{D+1}$ . Preferably, N and O are the smallest integers that effect the ratio N:O. [I threw this in for fun.]

15

Figure 2 is a flow chart that describes the first of the above described implementations. In block 200, a frame of data is received by the matching circuit 147. The frame may be received in any combination of serial and parallel modes. The frame comprises a series of ordered bits, from the first bit to the Lth bit. In block 204, the  
20 matching circuit 147 repeats the current frame M times, thereby creating LM bits. In practice, the matching circuit 147 will preferably not store LM bits but will process incoming bits serially, repeating a frame only after first puncturing that frame. For ease of discussion, however, it is assumed that the matching circuit has access to LM bits.

25

In block 206, the matching circuit 147 sets a counter C equal to P. In block 212, the next B bits of the frame (in this case the first B bits of the frame) are skipped and the next bit is deleted; C is also decremented. In block 214, the matching circuit 147 checks whether C is equal to  $P_D$ . If not, control passes back to block 212. Otherwise, control passes to block 216, where the next A bits are skipped and the next bit deleted; C is

decremented. Control passes to block 218, which checks whether C is 0. If not, control passes back to block 214. Otherwise, the matching circuit is finished.

Figure 3 is a flow chart that describes the second of the above implementations.

5 In block 300, a frame of data is received by the matching circuit 147. In block 310, the matching circuit 147 repeats the current frame M times, thereby creating LM bits. In block 312, the matching circuit 147 sets a counter C equal to 0 and a flag F to 0. In block 314, the next B bits of the frame (in this case the first B bits of the frame) are skipped and the next bit is deleted; C is also incremented. In block 316, the matching 10 circuit 147 checks whether the flag F has been set (i.e. is equal to 1). If the flag F has been set, control passes to block 318, which checks whether C is equal to P. If so, the routine exits. If not, control passes back to block 314. If the flag F has not been set, control passes to block 320, where the next A bits of the frame are skipped and the next bit is deleted; C is incremented. In block 322, the matching circuit 147 checks whether 15 C/2 is equal to P<sub>D</sub>. If so, the flag F is set in block 323 and control passes to block 318. If not, control passes to block 324, which checks whether C/2 is equal to or greater than P<sub>D+1</sub>. If so, control passes back to block 320. Otherwise, control passes back to block 314.

20 Figure 4 is a flow chart that describes the third of the above described implementations. In block 400, a frame of data is received by the matching circuit 147. The frame may be received in any combination of serial and parallel modes. The frame comprises a series of ordered bits, from the first bit to the Lth bit. In block 404, the matching circuit 147 repeats the current frame M times, thereby creating LM bits. In block 406, the matching circuit 147 sets a counter C equal to P and a flag F to 0. In block 412, the next A bits of the frame (in this case the first A bits of the frame) are skipped and the next bit is deleted; C is also decremented. In block 414, the matching circuit 147 25 checks whether F is set (equal to 1). If not, control passes to block 416, where a counter CX is set to N, where N is the nearest integer less than P<sub>D+1</sub>/ P<sub>D</sub>. The Flag F is also set to

1. Control passes to block 418, the next B bits are skipped and the next bit deleted; C and CX are decremented. Control passes to block 420, which determines whether CX is 0. If not, control passes back to block 418. If so, control passes back to block 412.

5        In block 414, if the Flag is set to 1, control passes to block 422, where a counter CX is set to 0, where O=N+1. The Flag F is also set to 0. Control passes to block 424, the next B bits are skipped and the next bit deleted; C and CX are decremented. Control passes to block 426, which determines whether CX is 0. If not, control passes back to block 422. If so, control passes to block 428, which determines whether C is equal to 0.

10      If so, the routine exits. Otherwise, control passes back to block 412.

The third implementation may also be implemented with the following C code, in which Pcnt is the count of the punctured symbols, Pidx(Pcnt) is the index into the unpunctured symbols of the Pcnt-th punctured symbol, for a given Pidx(0)

15      ( $0 < \text{Pidx}(0) < D+1$ ) and  $\text{Pcnt} > 0$ , and a counter RatioCnt is initialized to 0. After the first symbol is punctured, the following steps are repeated until  $\text{Pcnt} > P-2$ :

```
Pcnt++;
Pidx(Pcnt) += D;
RatioCnt += P_{D+1};
20      If RatioCnt >= P,
        RatioCnt = RatioCnt - P
        Pidx(Pcnt)++
Endif
```

25      Conclusion

Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

**WHAT IS CLAIMED IS:**

1. A method for decreasing the size of a frame of digital data from a first number of bits (LM) to a second number of bits (N), where the digital data comprising the frame is  
5 ordered from a first bit to an LMth bit, the method comprising the steps of:
  - (a) Receiving the frame;
  - (b) Deleting LM-N bits from the frame in a single iteration through the data,  
10 thereby creating a reduced length frame, wherein the deleting step is performed such that the distance between any two consecutive deleted bits within any group within a first subset of the frame is A bits, and the distance between any two consecutive deleted bits within any group within a second subset of the frame is B bits, where A is an integer greater than 0 and B is an integer greater than A, and where the first subset and the second subset  
15 together form a plurality of consecutive bits;
  - (c) Further processing the reduced length frame in a digital communications system.
2. The method of claim 1 wherein the frame consists of the first subset and the second subset.  
20
3. The method of claim 1 wherein B=A+1.
4. The method of claim 1 wherein A is equal to D-1, where D is the greatest integer less  
25 than LM/P, where P=LM-N.

5. The method of claim 1 wherein each of the first subset consists of the first N bits of the frame, where N is the length of the first subset.
6. The method of claim **Error! Reference source not found.** wherein the distance between consecutive deleted bits alternates between A and B throughout at least a portion of the  
5 frame.
7. The method of claim **Error! Reference source not found.** wherein the second plurality of bits consists of a first plurality of groups, each with a third number of bits, and a second plurality of groups, each with a fourth number of bits, wherein each group consists of a plurality of bits deleted in order, wherein the first and second plurality of bits are  
10 deleted according to a repeating sequence, the sequence consisting of all of the bits within one of the first plurality of groups, one of the first plurality of bits, and all of the bits within one of the second plurality of groups.
8. The method of claim 7 wherein:  
15 the third number of bits is equal to the lower bound of a first real number, where the first real number is equal to the number of bits within the second plurality of bits divided by the number of bits within the first plurality of bits; and  
the fourth number of bits is equal to the third number of bits plus 1.  
20 9. The method of claim 1 wherein the step of further processing the reduced length frame comprises the step of interleaving the reduced length frame.

ABSTRACT OF THE DISCLOSURE

REDACTED INFORMATION CONTAINED HEREIN IS UNCLASSIFIED  
DATE 10/20/2016 BY SP/SP/SP

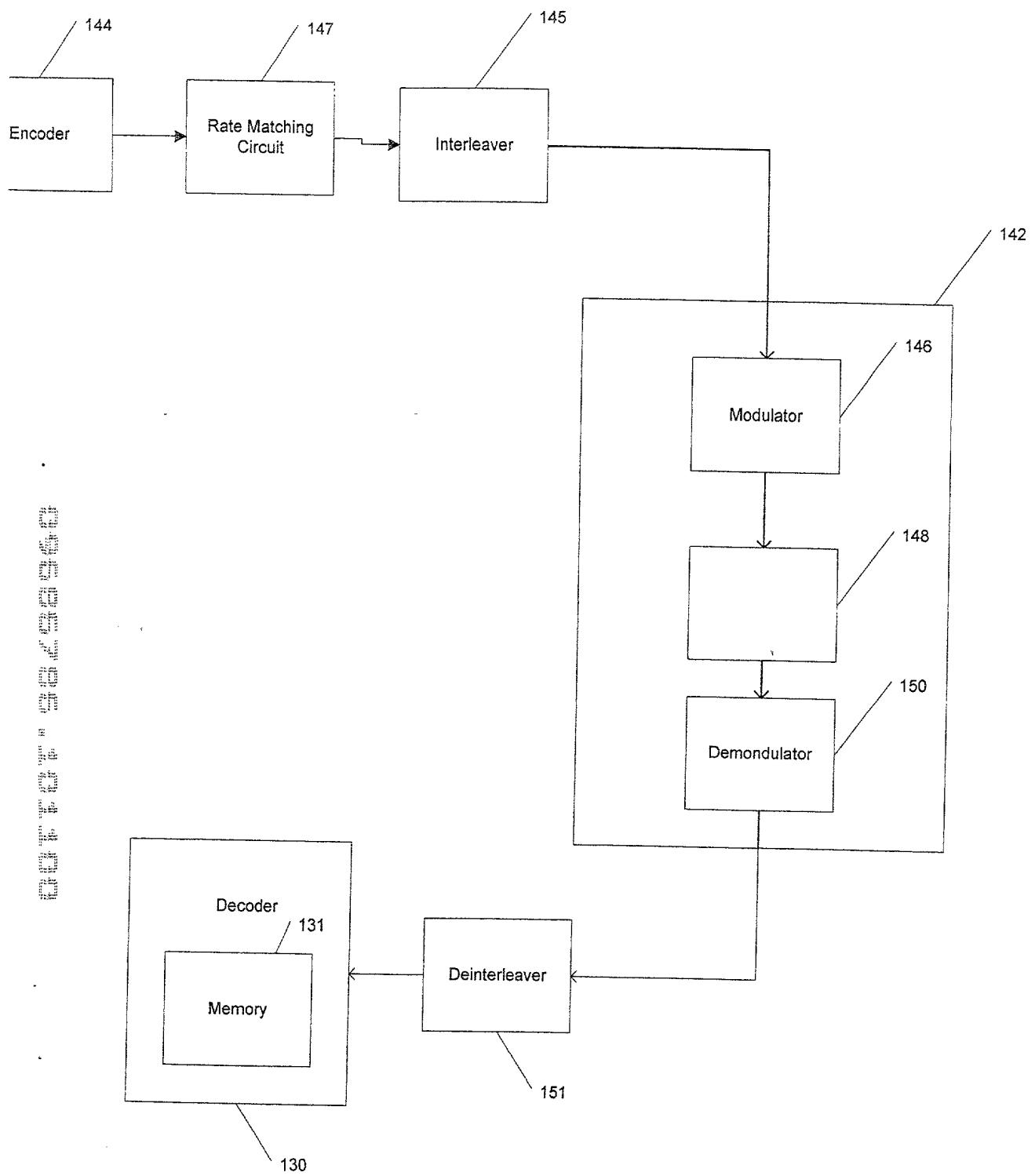


Figure 1

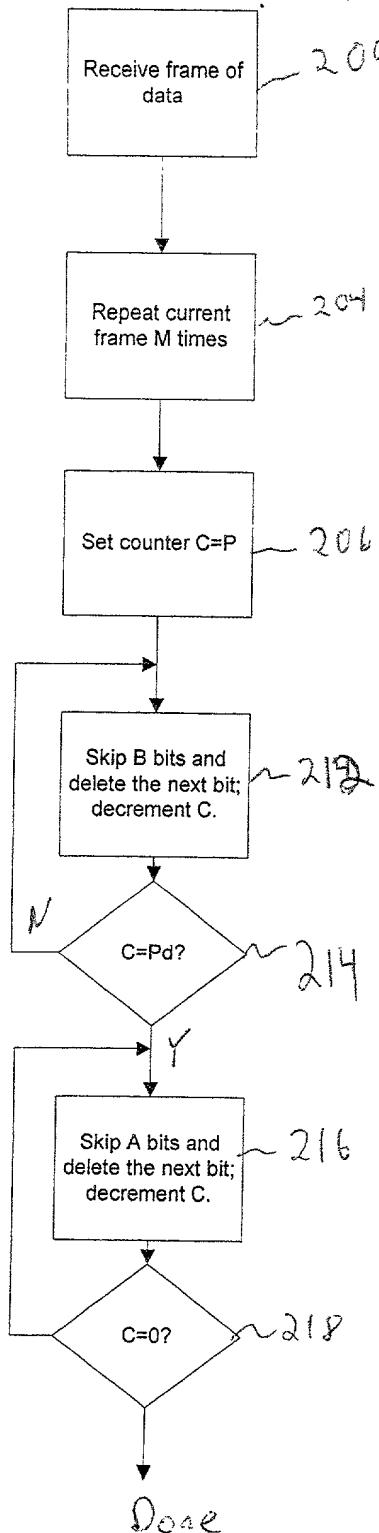


Figure 2

Figure 3

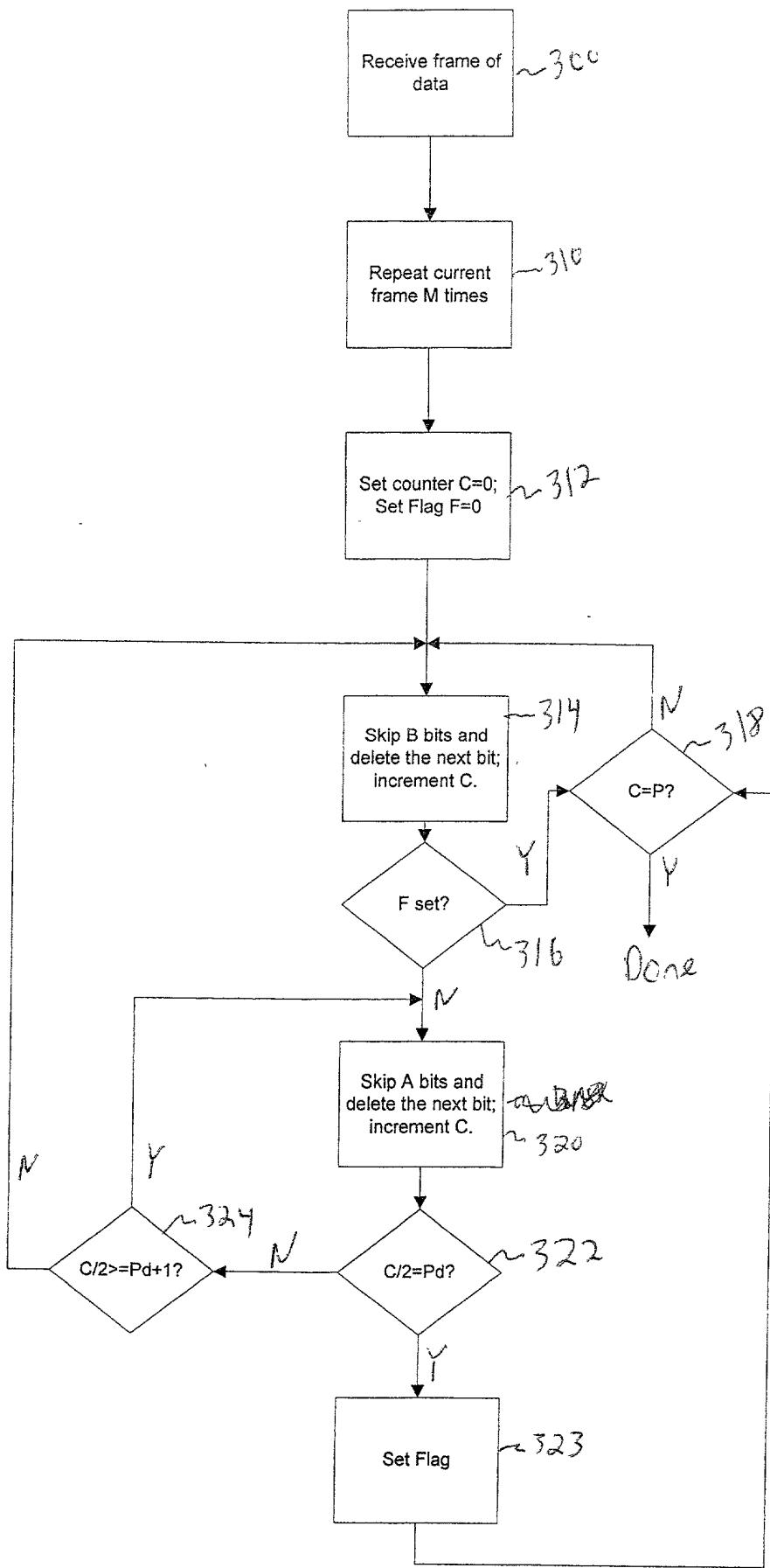
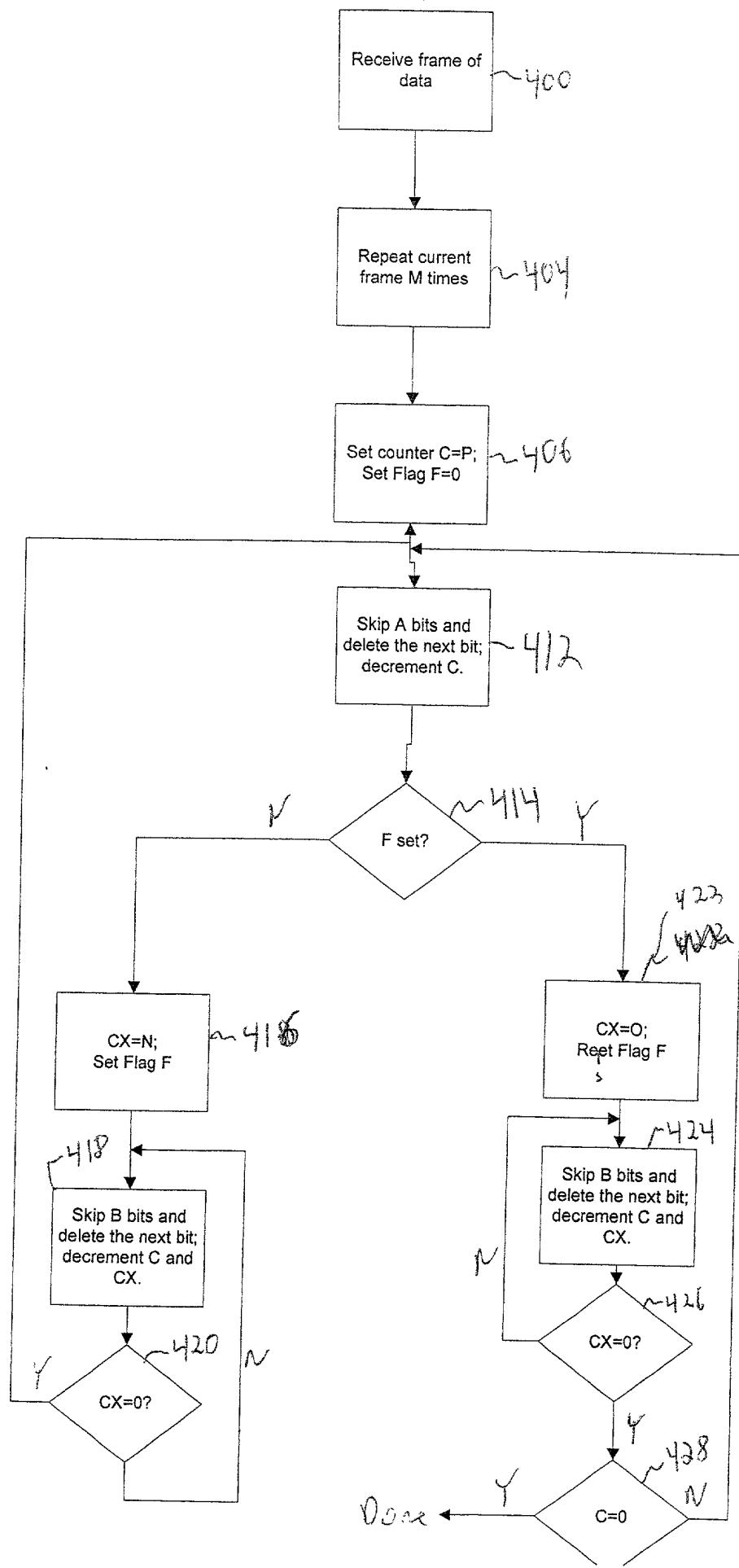


Figure 4



# Declaration, Power of Attorney, Correspondence Address, and Petition

Docket Number : 00-264

## Declaration

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

**I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:**

**Frame Matching Method**

**the specification of which was filed on and assigned a Serial Number 60/209,490.**

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

## Power of Attorney

I hereby appoint David G. Pursel, Reg. 28,659; Ralph R. Veseli, Reg. 33,807; Bruce R. Hopenfeld, Reg. 39,714; Gary Edward Ross, Reg. 29,431; Lloyd E. Dakin, Reg. 38,423; and Sandeep Jaggi, Reg. 43,331; as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and before competent international authorities.

## Correspondence Address

Please send all correspondence to:

LSI Logic Corporation  
Corporate Legal Department  
Intellectual Property Services Group  
1551 McCarthy Blvd., M/S D-106  
Milpitas, CA 95035  
Phone: (408) 433-8708  
Fax: (408) 433-7770

## Petition

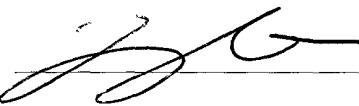
Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

# Declaration, Power of Attorney, Correspondence Address, and Petition

## First named inventor

First Name Feng

Last Name: Qian

Inventor's Signature: 

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Citizenship United States

Filing under seal does not preclude filing a motion for leave to file under seal if the Commissioner so directs.